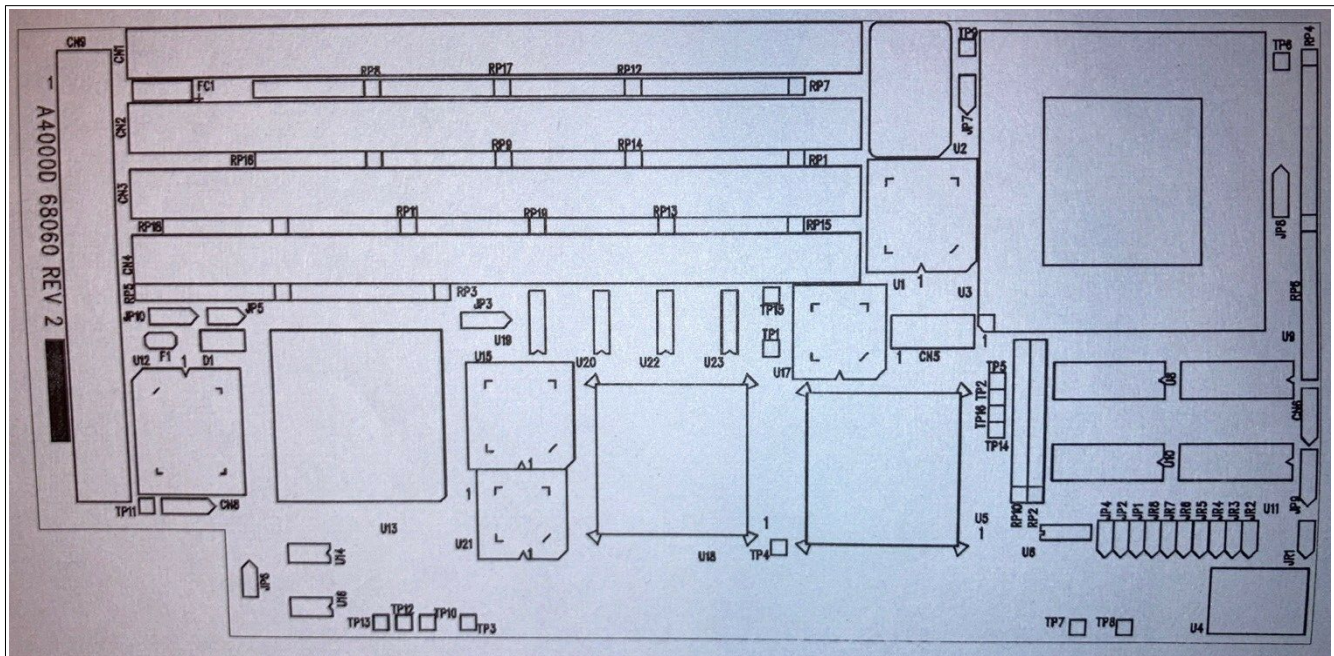


T-Rex II A4060DT Accelerator Jumpers and I/O Definitions

Updated: May 3, 2021 by Greg Donner



(Larger scale view on last page)

| |
|-----------------------------|
| A4000D 68060 Rev. 2 |
| Silkscreen (component side) |
| 17 20 |

Jumpers and I/O Definitions

| Jumpers | Definitions | Default |
|---------|--|---------|
| JP1 | CPU Select OFF = 68040/060 ON = Motherboard CPU | OFF |
| JP2 | Reserved | OFF |
| JP3 | Reserved | 1 and 2 |
| JP4 | Cache Burst to A4000 Motherboard OFF = Cache Burst Disabled ON = Cache Burst Enabled | OFF |
| JP5 | Interrupt Pending, DMA Backoffs ON = DMA Backoffs for Interrupt OFF = DMA Ignores Interrupt | OFF |
| JP6 | Active SCSI Termination ON = SCSI Termination Disabled OFF = SCSI Termination Enabled | OFF |
| JP7 | CPU Clock Disable (Test Only) ON = Clock Disabled OFF = Clock Enabled | OFF |

Jumpers and I/O Definitions (continued)

| Jumpers | Definitions | Default | | | | | | | | | |
|-------------|---|-------------|--------|--------|-------------|----------|-------------|------------|-------|--|-----|
| JP8 | CPU Clock 1 and 2 = 68040 2 and 3 = 68060 | | | | | | | | | | |
| JP9 | CPU Power 1 and 2 = 5V (68040) 2 and 3 = 3.3V (68060) | | | | | | | | | | |
| JP10 | EPROM Type 27C010 | 1 and 2 | | | | | | | | | |
| CN6 | 5V Fan (Not necessary for 68060) | | | | | | | | | | |
| CN8 | SCSI LED Indicator | | | | | | | | | | |
| JR1 | Memory Configured for Burst Mode ON = Burst Mode Support (Minimum of two SIMMs required) OFF = Non-Burst Mode (Support for any number of SIMMs) | ON | | | | | | | | | |
| JR2 | DRAM Speed versus CPU Clock <table style="width: 100%; border: none;"> <tr> <td style="text-align: center;">50 MHz</td> <td style="text-align: center;">40 MHz</td> <td style="text-align: center;">33 MHz</td> </tr> <tr> <td style="text-align: center;">OFF = 60 ns</td> <td style="text-align: center;">60/70 ns</td> <td style="text-align: center;">60/70/80 ns</td> </tr> <tr> <td style="text-align: center;">ON = 70 ns</td> <td style="text-align: center;">80 ns</td> <td></td> </tr> </table> | 50 MHz | 40 MHz | 33 MHz | OFF = 60 ns | 60/70 ns | 60/70/80 ns | ON = 70 ns | 80 ns | | OFF |
| 50 MHz | 40 MHz | 33 MHz | | | | | | | | | |
| OFF = 60 ns | 60/70 ns | 60/70/80 ns | | | | | | | | | |
| ON = 70 ns | 80 ns | | | | | | | | | | |
| JR3 | Burst Write Enabled ON = Write Enabled | ON | | | | | | | | | |
| JR4 | Burst Read Enabled ON = Read Enabled | ON | | | | | | | | | |
| JR5 | Memory Size OFF = 4 MB ON = 16 MB | OFF | | | | | | | | | |
| JR6 | Single/Double-sided SIMM OFF = Single-sided SIMM ON = Double-sided SIMM | OFF | | | | | | | | | |
| JR7 | Reserved | OFF | | | | | | | | | |
| JR8 | Refresh Mode OFF/ON = 4K Refresh (Asymmetrical) OFF = 2K Refresh (Symmetrical) Note: Both symmetrical and asymmetrical DRAMs are supported when JR8 is off. | OFF | | | | | | | | | |

Memory Location and Size Notes

Please note:

- CN1-CN4 are sockets for industry-standard SIMMs. All four sockets can support either 4 MB or 16 MB single-sided SIMMs, or 8 MB or 32 MB double-sided SIMMs, depending on the jumper settings of JR5 and JR6 as shown below.
- Burst will only function properly when there are *even multiples* of SIMMs installed.

JR5: OFF (Open), JR6: OFF (Open)

| | |
|-----|----------------------|
| CN1 | 8000000-83FFFFFF HEX |
| CN2 | 8400000-87FFFFFF HEX |
| CN3 | 8800000-8BFFFFFF HEX |
| CN4 | 8C00000-8FFFFFFF HEX |

JR5: ON (Closed), JR6: OFF (Open)

| | |
|-----|----------------------|
| CN1 | 8000000-8FFFFFFF HEX |
| CN2 | 9000000-9FFFFFFF HEX |
| CN3 | A000000-AFFFFFFF HEX |
| CN4 | B000000-BFFFFFFF HEX |

JR5: OFF (Open), JR6: ON (Closed)

| | |
|-----|----------------------|
| CN1 | 8000000-87FFFFFF HEX |
| CN2 | 8800000-8FFFFFFF HEX |
| CN3 | 9000000-97FFFFFF HEX |
| CN4 | 9800000-9FFFFFFF HEX |

JR5: ON (Closed), JR6: ON (Closed)

| | |
|-----|----------------------|
| CN1 | 8000000-9FFFFFFF HEX |
| CN2 | A000000-BFFFFFFF HEX |
| CN3 | C000000-DFFFFFFF HEX |
| CN4 | E000000-FFFFFFF HEX |

